Electronic Version
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Claims

[c1] 1.An antifuse device operable at a voltage thereacross, comprising:
(a)a first element having a first conductive region, a second conductive region and a tunneling region located between said first and second conductive regions, said tunneling region operatively configured so that a tunneling current is present between said first and second conductive regions of said first element when the voltage is applied across the antifuse device;
(b)a second element having a first conductive region, a second conductive region and a tunneling region located between said first and second conductive regions, said tunneling region operatively configured so that a tunneling current is present between said first and second conductive regions of said second element when the voltage is applied across the antifuse device; and
(c)an output node electrically coupled between said first element and said second element.

[c2] 2.An antifuse device according to claim 1, wherein the antifuse device has a programming state and further comprises a sensing circuit electrically coupled to said

output node, said sensing circuit operatively configured for sensing the programming state and outputting the programming state as a logic-level signal.

[c3] 3.An antifuse device according to claim 2, wherein said sensing circuit is a latchless sensing circuit.

[c4] 4.An antifuse device according to claim 1, wherein said sensing circuit consists essentially of an inverter.

[c5] 5.An antifuse device according to claim 1, wherein the antifuse device has an unprogrammed state and a programmed state and said output node has a corresponding unprogrammed voltage and programmed voltage when the voltage is applied across the antifuse device, the difference between said unprogrammed voltage and said programmed voltage being at least 400 mV when the voltage is 1 volt.

[c6] 6.An antifuse device according to claim 5, wherein the difference between said unprogrammed voltage and said programmed voltage being at least 700 mV when the voltage is 1 volt.

[c7] 7.An antifuse device according to claim 1, wherein said second element has an unprogrammed state and a programmed state, wherein in said unprogrammed state said tunneling region of said second element is essen-

tially non-conducting when the voltage is applied across the antifuse device and in said programmed state said tunneling region of said second element is conducting when the voltage is applied across the antifuse device.

[c8] 8.An antifuse device according to claim 7, further comprising a programming circuit operatively configured for changing said unprogrammed state to said programmed state.

[c9] 9.An antifuse device according to claim 8, further comprising an isolation element located between said first and second elements, said isolation element operatively configured to isolate said first element from said second element while said programming circuit is programming said second element.

[c10] 10.An antifuse device according to claim 1, wherein said tunneling region of said second element comprises a thin oxide layer.

[c11] 11.An antifuse element according to claim 10, wherein said tunneling region of said first element comprises a thin oxide layer.

[c12] 12.An antifuse element according to claim 11, wherein said thin oxide layer has an equivalent electrical thickness of no more than about 19 Å.

[c13] 13.An antifuse element according to claim 1, wherein each of said first and second elements is made from a semiconductor capacitor.

[c14] 14.An antifuse element according to claim 1, wherein each of said first and second elements is made from a semiconductor transistor.

[c15] 15.An antifuse device having an unprogrammed state and a programmed state, comprising:
(a)a bias element;
(b)a programmable antifuse element; and
(c)an output node electrically coupled between said bias element and said antifuse element so that said antifuse device forms a voltage divider;
wherein:
(a)when the antifuse device is in the unprogrammed state said bias element is operatively configured to be essentially non-conductive, and said programmable antifuse element is operatively configured to be essentially non-conductive; and
(b)when the antifuse device is in the programmed state said bias element is operatively configured to be essentially non-conductive, and said programmable antifuse element is operatively configured to be conductive thereacross.

[c16] 16.An antifuse device according to claim 15, wherein each one of said bias and antifuse elements is a thin-oxide device.

[c17] 17.An antifuse device according to claim 15, further comprising a sensing circuit, in electrical communication with said output node, operatively configured to sense the unprogrammed and programmed states of the anti-fuse device.

[c18] 18.An antifuse device according to claim 17, wherein said sensing circuit is a latchless circuit.

[c19] 19.An antifuse device according to claim 17, wherein said sensing circuit consists essentially of an inverter.

[c20] 20.An antifuse device according to claim 15, further comprising a programming circuit in electrical communi-cation with said programmable antifuse element and op-eratively configured to cause said programmable anti-fuse element to become conductive with said program-ming circuit is energized.

[c21] 21.A programmable antifuse device, comprising:
(a)a first element having a first conductive region, a sec-ond conductive region and a tunneling region located between said first and second conductive regions, said

tunneling region operatively configured so that a tunneling current is present between said first and second conductive regions of said first element when the voltage is applied across the antifuse device;

(b)a second element having a first conductive region, a second conductive region and a tunneling region located between said first and second conductive regions, said tunneling region operatively configured so that a tunneling current is present between said first and second conductive regions of said second element when the voltage is applied across the antifuse device; and

(c)a programming circuit in electrical communication with said second element and operatively configured to cause said tunneling region of said second element to become conductive when said programming circuit is energized.

[c22] 22.An antifuse device according to claim 21, wherein each one of said bias and antifuse elements is a thin-oxide device.

[c23] 23.An antifuse device according to claim 21, further comprising a sensing circuit, electrically coupled between said first and second elements, operatively configured to sense the conductive state of said second element.

[c24] 24.An antifuse device according to claim 23, wherein said sensing circuit is a latchless circuit.

[c25] 25.An antifuse device according to claim 23, wherein said sensing circuit consists essentially of an inverter.

[c26] 26.An antifuse device according to claim 21, further comprising an output node electrically coupled between said first and second elements and wherein the antifuse device has an unprogrammed state and a programmed state and said output node has a corresponding unprogrammed voltage and programmed voltage when the voltage is applied across the antifuse device, the difference between said unprogrammed voltage and said programmed voltage being at least 500 mV when a voltage of 1 volt is applied across said first and second elements.

[c27] 27.An integrated circuit chip, comprising:
(a)functional circuitry;
(b)at least one antifuse device operatively connected to said functional circuitry, said at least one antifuse device comprising:
(i)a first element having a first conductive region, a second conductive region and a tunneling region located between said first and second conductive regions, said tunneling region operatively configured so that a tunnel-

ing current is present between said first and second conductive regions of said first element when the voltage is applied across the antifuse device;

(ii)a second element having a first conductive region, a second conductive region and a tunneling region located between said first and second conductive regions, said tunneling region operatively configured so that a tunneling current is present between said first and second conductive regions of said second element when the voltage is applied across the antifuse device; and

(iii)an output node electrically coupled between said first element and said second element; and

(c)a programming circuit in electrical communication with said second element and operatively configured to cause said tunneling region of said second element to become conductive when said programming circuit is energized.

[c28] 28.An integrated circuit chip according to claim 27, further comprising a sensing circuit, electrically coupled between said first and second elements, operatively configured to sense the conductive state of said second element.

[c29] 29.An antifuse device according to claim 23, wherein said sensing circuit is a latchless circuit.

[c30] 30.An antifuse device according to claim 23, comprising a plurality of antifuse devices comprising a corresponding plurality of second elements comprising a corresponding plurality of tunneling regions, said programming circuit in electrical communication with said plurality of antifuse devices and configured to cause said plurality of tunneling regions to become conductive substantially simultaneously with one another when said programming circuit is energized.